INSTRUCTION MANUAL

DOVETRON MPC-1000R

TSR-500D/DAS-100

REGENERATIVE RTTY TERMINAL UNIT

DIGITAL AUTOSTART

E-SERIES

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MPC-1000R.400 and up.

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PREFACE

The Dovetron MPC-1000R Regenerative RTTY Terminal Unit normally consists of an E-Series Main Frame (Board Number A75100A-E), a TMS-100 AFSK Tri-Mode Tone Selector Assembly, a TSR-500D Signal Regenerator Board and a DAS-100 Digital Autostart Module.

When supplied with the TSR-500D/DAS-100 combination, the terminal unit provides Signal Regeneration, Speed Conversion with a 200 Character FIFO Buffer Memory, Keyboard-Controlled Word Correction and Digital Autostart.

The MPC-1000R is also available as a BASIC-R with a TSR Adapter (75156) which replaces the TSR-500D assembly, and functions as an MPC-1000C with a TMS-100 Tri-Mode Tone Selector.

If a TID-100 Station Identifier board is factory installed, it is mounted underneath the appropriate TSR assembly.

The KOS-100 Keyboard Operated Send option (if installed) is usually used in conjunction with a TID-100 assembly and is mounted underneath the TID-100.

A SCL-100 Selective Calling module may be plugged directly into the TSR-500D assembly for Sel Cal functions.

A PKC-100 Polar Keyer option is also available for use with Polar (double current) teleprinters.

With a TSR Adapter installed, the front panel Memory Empty LED is always lit and the Memory Function and Speed Selection switches are inoperative.

With the TSR-200D/TSR Adapter combination installed, the Signal and Loop Speed switches select the input and output baud rates of the TSR-200D Regenerator assembly.

The front section of this manual details the digital section (TSR-500D) of the terminal unit and the rear section (which is an MPC-1000C manual) details the mainboard section.

In case of conflict between the front and rear section of the manual, the information provided in the TSR-500D section should be considered correct.

OPERATING HINTS

MPC-1000R and TSR-500D

For the operator who prefers to turn on a new piece of equipment and read the manual later, the following is offered:

1) Remove the top lid and inspect the large-scale (LSI) integrated circuits and the four inter-connecting cables for a firm fit in their sockets. It is not unusual for transportation vibration to loosen them in their sockets.

2) Set the rear panel LOOP adjustment pot to midscale and check that the REGEN ON-OFF switch is in the ON position (UP).

3) Attach the power cord, teleprinter's loop line and an audio line from the receiver.

   A) Power cord should be grounded for safety and maximum performance.

   B) Teleprinter's loop line should NOT be grounded thru either loop jack. The teleprinter's loop line must be floating. If a three-way plug with a shield is used, insert it into the rear panel loop connector marked: 3-Way. The shield may be grounded to the terminal unit's cabinet.

   C) The input impedance of the MPC-1000R is 600 ohms, but the terminal unit may be driven with low impedance speaker audio lines, provided the audio is turned up high enough. Many receivers have phone patch or anti-vox outputs, which are usually in the 500 to 2500 ohm region and they make ideal audio sources for the terminal unit.

4) Place all the front panel toggle switches UP, except the Autostart/Motor Control switch. Place it in the Motor ON position.

5) Set the LEVEL control to 9 o'clock and the THRESHOLD control to 12 o'clock.

6) Set the MODE switch to MS, which is the proper position for normal In-Band Diversity operation.

7) Adjust the Mark and Space VFOs to the desired tone frequencies.

8) Set the SIGNAL Speed Switch to the anticipated speed of the incoming signal.

9) Set the LOOP Speed Switch to the speed of the local teleprinter. (45 Baud = 60 WPM, 75 Baud = 100 WPM, etc.)

10) Tune in a known RTTY signal, peaking the Mark and Space VFOs for maximum amplitude of the horizontal and vertical CRT traces and start copying. If the copy is garbled, reverse the NORMAL/REVERSE switch.

11) Now sit back and read the rest of this manual and discover how easy it is to implement all the operating features and functions.

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MPC-1000R REGENERATIVE RTTY TERMINAL UNIT

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SECTION I - DESCRIPTION

The MPC-1000R Regenerative RTTY Terminal Unit is basically an MPC-1000C Multipath-Diversity RTTY Terminal Unit with a TSR-500D Teleprinter Speed Converter-Regenerator mounted internally to provide Signal Regeneration, Speed Conversion, up to 200 characters of Silastic Buffer Storage and keyboard-controlled Word Correction.

The front panel contains switches for basic control of the regeneration, speed conversion and memory exercising functions.

Rear panel connectors permit remote control of the other functions, such as Phasing On-Off, Word Erase, etc.

The Word Correction function is automatic and keyboard-controlled via internal circuitry that is capable of recognizing the SPACE and BLANK characters generated by the local teleprinter.

In addition, the MPC-1000R contains a TMS-100 Tri-Mode AFSK Tone Selector assembly, which permits front panel selection of one of three different Mark-Space-Shift combinations that have been preset for the AFSK Tone Keyer.

All other front panel controls perform in the same manner as their counter parts on the MPC-1000C.

For this reason, the E-Series manual for the MPC-1000C pertains to the MPC-1000R unless specifically noted in the following paragraphs or on the accompanying MPC-1000R prints and schematics.

When the rear panel REGEN ON-OFF switch is in the OFF position, the TSR-500D Regenerator assembly is inhibited, and the MPC-1000R functions as an MPC-1000C. With this switch OFF, the TSR-500D may be removed for service and the terminal unit continued to be used as a non-regenerating modem.

When the REGEN ON-OFF switch is in the ON position, all incoming and outgoing signals (except Mark-Space Reversals from the RY Generator) are regenerated to less than 0.5% bias distortion.

Since the input and output baud rates of the Regenerator may be controlled by the front panel speed switches, and may be set to different speeds, the Regenerator section may also be used as a simultaneous up-down speed converter.

A silastic buffer storage section prevents character over-runs during Down-Speed Conversion, and may be Preloaded and Recirculated.

This buffer memory section consists of five 40 character FIFO buffer elements for a total storage of 200 characters.

SECTION II - THEORY OF OPERATION

The TSR-500D Teleprinter Speed Converter-Regenerator is a digital device that performs Signal Regeneration, Up-Down Speed Conversion, Buffer Storage, Word Correction, Phasing Pulse Generation (BLANK or LTRS) and Variable Character Rate Control.

These functions are accomplished thru the use of a pair of Universal Asynchronous Receiver/Transmitters (UARTs), First-in First-out (FIFO) Silastic memory chips, a crystal-controlled oscillator and various logic and switching elements.

The crystal-controlled oscillator operates at 60 KHz and uses a tuning-fork type piezoelectric quartz crystal.

The output of this oscillator is divided down by two separate BCD/N stages which are switch controllable and provide the two separate clock frequencies required by the UARTs for up-down speed conversion.

The Signal Speed clock is Clock 1 and the Loop Speed clock is Clock 2.

With the MPC-1000R in Receive and the Memory section in Operate, Clock 1 drives the Input register and Clock 2 drives the Output register of Uart 1. When the TU is switched to SEND, the two clocks are reversed.

If the two clocks have been set to the same frequency, that is, the same speed, UART 1 functions solely as a regenerator.

When the two clocks are set for different speeds, the UART also functions as a speed converter, because it is outputting the data at a different speed than it took it in at.

When the MPC-1000R is in SEND-Recirculate (as when calling CQ from the preloaded memory), both the input and output registers of UART 1 are being driven by Clock 1, the Signal Speed clock.

When in RECEIVE-Preload, the output register is not permitted to output, because the memory is being deliberately loaded-up.

For this reason, a second UART has been implemented in the TSR-500D. Its input clock is <u>always</u> Clock 1 (Signal Speed) and the output clock is <u>always</u> Clock 2 (Loop Speed). Since the Loop Speed is identical to the local teleprinter's Baud rate, UART 2 provides local copy even when the TSR-500D is Recirculating or Preloading at Signal Speed.

A Memory Hold circuit (three elements of U25) has been incorporated which permits the local teleprinter to receive an incoming message via UART 2 when the Memory is recirculating.

This permits the operator to Preload the Memory with a CQ (or any other message), and to switch the TU to SEND-Recirculate, which will repetitiously transmit the contents of the Memory over and over again.

At the end of the transmission, the TU may be switched to Receive, leaving the Memory intact (still in Recirculate), and receiving an incoming answering signal, without loosing the Preloaded message.

If no answer is received, the TU may be switched back to SEND and it will immediately resume sending the originally Preloaded message.

If an answer is received, when the TU is switched back to Send, the Memory is simply cleared with the front panel CLEAR switch and the Memory switched to OPERATE.

Whenever the MPC-1000R is in RECEIVE, the Space-shift feature of the Word Correction circuit is inhibited by CR13 and the Input FIFO will always function as part of the main memory.

The Blank Erase circuit in Receive is also inhibited (when it is necessary to do so), because when the main memory section fills, it will enable the TD Inhibit circuit which in turn inhibits the Blank Erase circuit via CR15.

In other words, in Receive, with five FIFOs, a full 200 character buffer memory is provided.

The Dual One-Shot (U22) provides the automatic Variable Character Rate Control and functions only in SEND. It also provides the logic for the Phasing Pulse circuit, which only operates when the TU is in SEND and the Memory section is empty.

The BLANK and LTRS character generation is accomplished by pulling the tri-state output lines of FIFO 1 (OUTPUT FIFO-U4) either to ground or up to +5 volts thru the 4.7K resistors at R40 thru R47. These FIFO lines automatically go to tri-state when the Memory is empty.

As supplied by the factory, the BLANK character is enabled. LTRS character may be generated by removing the jumper AB and installing a jumper or 15 ohm resistor at AC.

The BLANK "diddle" is preferable, because it will not affect the FIGS or LTRS state of the receiving teleprinter.

A LTRS "diddle" may interfere with a slow typist's ability to send a FIGS character and then a numeral. If the LTRS character is automatically inserted by the diddler between the FIGS and the numeral, the receiving teleprinter will be back in LTRS case by the time the numeral character arrived, and the character Y

would be printed instead of the numeral 6, etc.

The LTRS character generation mode has been incoroporated on the TSR-500D for commercial and military users that require an automatic SPACE pulse (Start) to be sent during Marking periods to phase crypto equipment.

Other options on the TSR-500D are the inverters provided on the input and output lines. Jumpers have been provided to permit easy inversion of these signal lines when interfacing the TSR-500D to other types of data modems.

The Memory Clear line (J1-1) is connected to the front panel Memory Clear switch and clears all five FIFOs. The Word Erase line (J2-7) goes to a rear panel connector (Word Erase) and only clears the Input FIFO. A contact closure to ground at this connector will provide Word Erase and has been provided for users of teleprinters that do not have a keyboard BLANK button. Automatic Memory Clear is provided by C20.

If the UARTs have been programmed for Stop Bit NOT Required (SBR switch S3 set to NO), breaking the local loop line with the keyboard BREAK line will also provide WORD ERASE. But breaking the loop via the BREAK key will also let the local typing unit run open and possibly print garble. A separate Word Erase button is probably preferable.

If the rear panel Word Erase connector is not being used, this connector may be converted to a Space Cal line by removing Jumper X2 and installing Jumper X1 on the TSR-500D board.

This Space Cal line may also be used as a full-shift CW-ID connector.

If the TID-100 Station Identifier has been coded for Baudot or ASCII code generation (as used in an Answer back mode), the open-collector output of the IDer may be connected to this Space Cal line.

Most TSR-500D assemblies are factory-supplied with 5 FIFOs, i.e., 200 characters of storage.

FIFOs U4 and U8 are always installed and provide the minimum 80 characters of storage.

If any of the optional FIFOs (U5, U6 or U7) are not installed, ten jumpers or low resistance resistors are installed in lieu of the missing FIFO and socket. These locations are detailed on print 75142, upper right corner.

Additional FIFOs may be field-installed in any of these locations by removing the ten jumpers and installing a socket and a Fair-

child 33511 or 33512 FIFO package.

To break-out the parallel data lines between the Input and Output registers of Uart 1 (for routing to some other peripheral device, such as a processor or additional memory), replace FIFO U5 or U6 with a 28 pin/cable assembly, or hard-wire directly to the jumper locations under the socket.

Code Conversion peripherals will not function properly with the TSR-500D, because the input and output registers of both UARTs are always set to the same coding level by NB-1 and NB-2 of the UART Program switch S3.

Although all logic elements in the TSR-500D are CMOS, they are fully-buffered to interface with TTL logic.

When interfacing to other CMOS circuits that are operating at higher levels, such as +12 or +15 volts, remember that Q1 is switching between zero to +5 volts.

The keyboard-controlled Word Correction circuit has been implemented at the Input FIFO (U8).

Whenever the MPC-1000R is in SEND, this Input FIFO stores the data from the local keyboard or Tee Dee. When it receives a SPACE character from the local teleprinter (which would normally be sent at the end of a word), the Input FIFO releases the word into the next FIFO (U7) and the word ripples down thru the memory to the first open location.

SPACE character recognition is accomplished in U12.

If an incorrect or mis-spelled word has been entered into the Input FIFO, it may be erased by sending a BLANK character from the local teleprinter.

BLANK character recognition is accomplished in U13.

The main memory section may contain one, two, three or four 40 character FIFO elements (U4 thru U7). Whenever the last FIFO in this section is filled, the Input FIFO (U8) is brought on-line as an over-flow FIFO, which adds 40 additional characters of storage to the main memory section.

Word Correction is automatically inhibited when the Input FIFO is in the Over-Flow mode and is accomplished by CR14 and CR15.

These diodes are tied back to the Set-Reset latch circuit in the Tee Dee Inhibit circuit, which in turn, is enabled when the last FIFO in the main memory section is filled.

For example, with 5 FIFOs installed, the Tee Dee Inhibit circuit is enabled when 160 characters have been stored, but the fifth FIFO comes on-line and lengthens the memory to 200 characters. This effectively prevents lost characters from overfilling the Memory, because at the same time the TD Inhibit circuit is enabled, the Variable Character Rate circuit is inhibited and the output character rate is raised to machine-speed.

The length of time that the character rate is maintained at machine speed is controlled by the time-constant of C17, R76 and R77. The factory installed values permit the memory to be emptied out at machine speed before the character rate is smoothly (not abruptly) lowered back to the preselected character rate.

The front panel Memory FULL LED lights when 160 characters have been stored and stays lit while the memory is outputting at machine speed.

The Word Correction circuit may be completely inhibited at all times by adding a jumper at location X2, which defeats the Space Character recognition circuit and removing the diode at CR2, which defeats the BLANK character recognition circuit.

With the Word Correction circuit disabled in this way, all the FIFO storage elements in the TSR-500D function as standard FIFOs in both SEND and RECEIVE.

An inversion scheme has also been provided on the control line (J1-8) that switches the TSR-500D between Receive and Send.

When installed in an MPC-1000R terminal unit, R62A and CR8 are installed and R62B and CR9 are omitted. This permits a zero signal (provided by pull-down resistor R61) to keep the TSR-500D in Receive until a +5 to +15 volts is applied by J1-8.

For other control applications, R62B and CR9 may be installed in place of R62A and CR8, in which case, the Control Line is pulled-high thru R63 and inverted by U24, putting the TSR-500D into Receive. A ground at J1-8 pulls the line low, which is inverted to a high state by the inverter U24, putting the TSR-500D into SEND.

Double inverters are used as LED drivers (DS1 and DS2) and assure full brilliance of both the front panel and board mounted LEDs.

Although the FIFO FULL line has been brought out from each FIFO in the J2 (rear) cable, they are not used when the TSR-500D is installed in an MPC-1000R.

Their primary purpose is to indicate the status of each FIFO (Full

or Empty) when the TSR-500D is used as a support element in a peripheral-type piece of equipment.

These lines are normally high (+5 volts) when the FIFO is empty and go to zero when the FIFO fills.

The five lines may be buffered (and inverted) thru a single hex inverter (such as the 14069) and used to drive individual LED indicators.

They may also be used to drive a digital to analog converter circuit, which in turn would easily drive an analog meter which would indicate the amount of storage, i.e., 20%, 40%, 60%, 80% and Full.

INTERNAL LOGIC - UART #1/MEMORY SECTION and UART #2 SECTION

The output register of UART 2 is always clocked at the speed set by the LOOP SPEED switch and provides local teleprinter copy when UART 1 and its memory section are being clocked at the speed set by the SIGNAL SPEED switch.

MEMORY	RECEIVE	SEND
OPERATE MODE	200 characters of FIFO memory. Word Correction circuits are disabled. Local teleprinter is driven by UART 1 and the Memory section. If down-converting, the Memory Full LED will light when 160 characters have been backed up in the memory section. Normally, the Memory EMPTY LED will be lit, since the OPERATE mode is usually set for straight-thru or up-conversion of the baud rate.	200 characters of FIFO memory. Word Correction is enabled and Input FIFO functions as a word-storage element that transfers a complete word to the main memory upon receipt of a Space character, or erases the complete word upon receipt of a Blank character. Memory Full LED lights on 160th character indicating only 41 characters of storage remaining (40 FIFO + 1 UART character), Input FIFO comes on-line as an over-flow storage element, Word Correction is inhibited, and Character Rate is automatically raised to machine speed until memory has been emptied. When Memory Full LED extinguishes, Word Correction is re-enabled and output speed returns to preset Character Rate. Local copy is provided by local keyboard.
PRELOAD MODE	200 characters of memory. Memory Full LED lights on 160th character, indicating only 41 characters of unused memory remain. Local printer is driven by UART 2 and prints what is being preloaded into the Memory Section by UART 1. Word Correction is disabled.	200 characters of memory. Word Correction is inhibited at 160th character and input FIFO comes on-line as over-flow FIFO when Memory Full Led is lit. Local copy is provided by the local keyboard.
RECIRCULATE MODE	Local printer is driven by UART 2 and provides local copy of recieved signals. This mode permits receiving an answer to a CQ without having to switch to Operate which would run out preloaded memory.	Local copy via UART 2 while UART 1 and Memory section are being recirculated at Signal Speed. Provides up-conversion when Signal Speed is less than LOOP Speed.

SECTION III - FRONT PANEL CONTROLS

AFSK SWITCH

The three positions of the AFSK Tone Keyer Switch (A, B & C) select the pre-set Mark and Space tones that have been calibrated into the tone keyer via the rear panel tone keyer calibration pots. Each pot is a 20 turn cermet potentiometer of infinite resolution and has a clutch action at the end of travel. Over-running the pot during calibration will not damage it.

To calibrate the Space tone, turn the REGEN ON-OFF switch to OFF, and remove the LOOP fuse, which breaks the loop line. This forces the AFSK tone keyer into Space. The Loop may also be opened by depressing the local teleprinter's Break button.

REGENERATOR/MEMORY SECTION SWITCHES

The SIGNAL and LOOP Signal Speed switches are calibrated in Baud. Each switch controls an independent BCD/N divider section that is driven by a common crystal-controlled oscillator.

The SIGNAL switch should be set to the baud rate of the RTTY circuit. The LOOP switch should be set to the baud rate of the local teleprinter. It is generally advantageous that the local teleprinter be operated at a baud rate equal to or faster than the fastest baud rate signal to be received.

The Memory section is controlled by two front panel toggle switches. These switches are labelled CLEAR-UNLOAD and OPERATE-PRELOAD-RECIRCULATE.

The CLEAR-UNLOAD switch is normally in its center-off position. When lifted to CLEAR, this switch immediately dumps the contents of the entire memory.

When lowered to the UNLOAD position, the preset Character Rate is increased to machine speed and the FULL LED indicator lights.

During this period (FULL LED lit), the Tee Dee INHIBIT circuit is enabled and permits an external relay to open the solenoid circuit of a tape-pulling TD, thus preventing character overruns during down-conversion of the baud rate.

This UNLOAD action is also automatically enabled whenever the last FIFO element in the main memory section is filled.

During normal operation, the OPERATE-PRELOAD-RECIRCULATE switch is left in the OPERATE position.

Moving the switch to PRELOAD permits the Memory Section to accept and store RTTY signals, either from the incoming signal (Receive) or from the loop (Send).

When Preloading in the Receive mode, a second UART (U2) provides regeneration and speed conversion from signal speed to loop speed and premits local copy.

In the RECIRCULATE position, the contents of the Memory are recirculated in UART #1 (U3) at Signal speed if in Send and at Loop speed if in Receive.

When recirculating the memory in Send, the second UART again provides local copy.

During normal (OPERATE) operation, the EMPTY LED will be lit, indicating that the incoming signal is flowing thru the Memory and not being stored.

If down-converting (i.e., copying a 50 Baud signal on 45.45 Baud teleprinter), this LED will extinguish as the Memory starts to store the over-runs, and will light again when the incoming signal "marks" long enough for the Memory to empty out.

In the Send mode, if the Character Rate has been set to something less than machine speed, a fast typist will be able to enter data into the Memory faster than it will be taken out.

If the Memory is filled, the FULL LED will light, indicating that the Input FIFO is absorbing the momentary overflow, that the slower Character Rate has been increased to machine speed and that the Tee Dee Inhibit Circuit has been enabled.

At the end of the machine speed emptying-out period, the FULL LED will extinguish and the Character Rate will drop smoothly (not abruptly) back to its preset, slower than machine speed Character Rate.

SECTION IV - PROGRAMMING THE REGENERATOR SECTION

Assuming that the MPC-1000R/TSR-500D is to be used for Radio RTTY communication (5 level Baudot), program the UARTs via the 8 pole DIP switch (S3):

SWITCH POLE	FUNCTION	MODE	SWITCH POSITION
8	NB1	Zero	LEFT
7	NB2	Zero	LEFT
6	TSB	1.5	RIGHT
5	SBR	NO	LEFT
4	PRTY	NO	LEFT
3	RPT	NO	RIGHT
2	PHSG	OFF	LEFT
1	PRLD	YES	RIGHT

UART CODING (NB-1 & NB-2) POLE 8 & 7

The Regenerator Section of the TSR-500D consists of a pair of Universal Asynchronous Receiver/Transmitters (UART), which may be programmed for 5, 6, 7 or 8 level codes via poles 7 and 8 of Switch S3.

These poles are identified as NB-1 and NB-2. The coding chart for NB-1 and NB-2 is etched on the PC board. For five level Baudot coding, NB-1 and NB-2 are both switched to ZERO (LEFT).

TOTAL STOP BITS (TSB) POLE 6

When programmed for a five level code, some UARTS permit the total number of Stop Bits to be set to 1.5, instead of the more common 1.0 or 2.0 character units.

This permits a character unit coding of 7.5, instead of 7.0 or 8.0.

The TSR-500D has been designed with an Automatic Stop Bit Length Select circuit.

When Pole 6 is programmed to the RIGHT for a 1.5 CU Stop Bit, the UARTs are programmed for a 1.5 CU Stop Bit when the TSR-500D is in SEND and for a 1.0 CU Stop Bit when the TSR-500D is in RECEIVE.

Selecting Pole 6 to the LEFT provides a 1.0 CU Stop Bit in both Send and Receive.

To permit a 1.5 CU Stop Bit in both Send and Receive, remove the diode directly below the U3 UART and change the 100K resistor at R39 to a 10K, 5% resistor.

RECEIVED STOP BIT REQUIRED (SBR) POLE 5

Switch pole 5 sets the SBR (Stop Bit Required). Normally, it is best to leave this function in the NO position. There is no reason to force the UART to dump a good character just because the Stop Bit was not detected.

With the high redundancy of the English and Spanish languages, it is always better to print a character, even if it is wrong, because the automatic Stop Bit generated by the UART will prevent the local teleprinter from losing signal synchronization.

PARITY SELECT (PRTY) POLE 4

Switch pole 4 permits selection of PARITY, a function not normally used in Radio TTY communication. This switch should be left in the NO position.

If Parity is required, consult the manufacturer's spec sheet on the particular UART installed in the TSR-500D.

Most Uarts select Parity in the following way:

NP	ESP	MODE
Ø	Ø	ODD
Ø	1	EVEN
1	Ø or 1	NO

PRELOAD AND RECIRCULATE (PRLD & RPT) POLE 3 & 1

Switch poles 1 and 3 provide Preloading and Recirculation of the Memory section. Since these positions are over-ridden by the front panel toggle switches, both of these switches MUST be in the RIGHT position: REPEAT-NO and PRELOAD-YES.

PHASING (BLANK-LTRS) PULSES (PHSG) POLE 2

Programming the PHASING function ON will provide an automatic generation of the BLANK character when the MPC-1000R is in SEND and the Memory section is empty. This BLANK character may be changed to a LTRS character by removing the jumper in the BLANK location and inserting a 15 ohm resistor in the LTRS location just to the right of it.

The BLANK character has an advantage over the LTRS character, since the case state (FIGS or LTRS) of the receiving teleprinter will not be changed by receipt of the BLANKS character.

The LTRS character option has been provided for commercial users that require Phasing Pulses (single Start pulses) during periods of inactivity to maintain synchronization of their crypto equipment.

The PHASING option (BLANKS or LTRS) may be inhibited entirely by switching Pole 8 of the UART program switch to OFF (LEFT) position or by grounding the rear panel PHASING connector. It is automatically inhibited when the MPC-1000R is in the REC mode or when the TID-100 is enabled.

The repetition rate of the BLANK (or LTRS) character is determined by the setting of the CHARACTER RATE adjustment pots. One pot is board-mounted on the TSR-500D assembly and the other is on the rear panel of the MPC-1000R.

VARIABLE CHARACTER RATE (R74)

Character Rate is normally set for some rate less than machine speed.

Its sole purpose is to lengthen the Stop Bit duration of each regenerated character as it is transmitted, smoothing out the signal at the receiving teleprinter. This slower character rate does not change the basic baud rate of the outputted signal.

As an example, a 45.45 Baud signal that normally has a speed of 60 WPM (at machine speed), may have its Character Rate slowed to 40 or 45 WPM by merely lengthening the stop pulse on the end of each character.

A dual one-shot circuit at U22 provides this "long stop" pulse.

With a slower character rate, the main memory section may be filled more easily, and should this happen, the Character rate is automatically increased to full machine speed.

At the same time, the Input FIFO element that normally provides Word Correction comes on-line as an overflow FIFO and its entire 40 character storage may be used in the normal mode.

When this condition occurs, the front panel FULL LED will light, indicating to the operator that he has filled the main memory and is outputting the stored data at machine speed.

It also indicates that if he is inputting at a faster rate than the output rate and that the Input FIFO has come on-line as an overflow buffer.

Whenever the FULL LED is lit, the TEE DEE Inhibit circuit is also enabled and may be used to inhibit a tape pulling Tee Dee or to provide an aural or visual alarm.

NOTE: If any difficulty is experienced with dropping an occasional character while recirculating at machine speed, increase the value of R73 (20K) to 27K. This will slow down the spoon-feeding rate of the Dual One-Shot U22 when operating at machine speed.

This is also an effective way of stretching the time duration of the Stop Bit and may be used to generate long Stop Bits should the requirement arise. The higher the value of R73, the longer the Stop Bit will be. A 27K resistor at R73 will provide a Stop Bit length of approximately 2.0 when putputting at machine speed.

SECTION V - DUAL CLOCK

The dual-clock is crystal-controlled at 60.000 KHz. Two identical divider sections divide this frequency down to those frequencies required by the UART's input and output clock ports for operation at the various Baud rates.

The front panel speed select switches are calibrated in terms of Baud:

SWITCH CAL	ACTUAL BAUD	SPEED - WPM
45	45.45	60 (61.3)
50	50.00	66.6
57	56.88	75
75	74.2/75.0	100/106
110	110.00	100/ASCII

When the MPC-1000R is in REC, Clock 1 provides the SIGNAL speed clock frequency to the input clock port of the UART regenerator (U3). Clock 2 provides the LOOP speed clock frequency to the output clock port.

When the MPC-1000R is switched from REC to SEND (locally or remotely), Clock 1 and Clock 2 are interchanged at the UART by the bilateral steering section. The input and output data lines are also interchanged at the Uart's data ports simultaneously.

This switching action permits an incoming signal to be up-converted to a faster teleprinter during REC, and the teleprinter's faster keyboard signal to be down-converted to the slower signal rate during SEND.

SECTION VI - TEST POINTS (TSR-500D)

Test points have been provided on the TSR-500D assembly to aid in trouble shooting.

TP-1: CRYSTAL OSCILLATOR OUTPUT

The oscillator circuit is comprised of a Statek "tuning-fork" type quartz crystal and a CMOS 4007 dual complementary pair plus inverter. This type of oscillator requires very low current and often requires two or three seconds to start oscillating after turn-on. The nominal frequency of the crystal is 60.000 KHz ±0.05%.

TP-2: CLOCK 1 OUTPUT

The frequency at TP-2 is the output of the BCD/N dividers U18 and U19 as programmed by the SIGNAL Speed Select switch located at S1.

TP-3: CLOCK 2 OUTPUT

The frequency at TP-3 is the output of the BCD/N dividers U20 and U21 as programmed by the LOOP Speed Select switch located at S2.

Clock 1 and Clock 2 should output the following frequencies, depending on the setting of their respective speed switches:

45 Baud (60 WPM)	732 Hz.
50 Baud (66 WPM)	800 Hz.
57 Baud (75 WPM)	909 Hz.
75 Baud (100 WPM)	1200 Hz.
110 Baud (100 WPM ASCII)	1765 Hz.

TP-7: UART INPUT CLOCK

The frequency at TP-7 is the Input Clock to UART #1 (U3) at the output of the bilateral steering section. In REC, it is Clock 1 and in SEND it is Clock 2.

TP-4: UART OUTPUT CLOCK

The frequency at TP-4 is the output Clock to the UART (U3) at the output of the bilateral steering section. In REC, it is Clock 2 and in SEND it is Clock 1.

In PRELOAD, TP-7 and TP-4 will both have Clock 1 signals when the MPC-1000R is in REC. When in SEND, both test points will have Clock 2 signals.

In RECIRCULATE, both test points will have Clock 2 in REC and CLOCK 1 when in SEND.